CLAIMS:

1. A circuit module comprising a first and second sub-circuit and a communication link coupled between the first and the second sub-circuit, the sub-circuits being arranged to communicate signals via the communication link during operation;

- the sub-circuit comprising a version number memory for storing a version number, the sub-circuit providing a performance dependent on the version number that is stored in the version number memory;
- the second sub-circuit comprising a write-protected memory and a version number control circuit arranged to send update values for the version number memory from the write-protected memory via the communication connection.

2. A circuit module according to Claim 1 wherein the circuit module is a multi-component module, comprising a package that contains the first sub-circuit in a first integrated circuit and the second sub-circuit in a second integrated circuit.

3. A circuit module according to Claim 1 wherein the control circuit is arranged to send the update values multiplexed with normal operating signals that are communicated between the first and the second sub-circuit.

4. A circuit module according to Claim 3 wherein the communication connection is a communication bus coupled to the sub-circuits, the first sub-circuit being arranged to support execution of commands received via the communication bus, including an update command for updating the version number in the version number memory; the circuit module comprising:

- an external bus input;
- the version number control circuit being a watchdog circuit coupled between the external bus input and the communication bus, the watchdog circuit being arranged to pass commands from the external bus input to the communication bus conditionally, the watchdog circuit detecting whether the update command to update the version number is

received and if so to pass said update command, replacing a version number in the update command by a version number from the write protected memory.

5. A circuit module according to Claim 4, comprising a processor integrated circuit containing a CPU and the write-protected memory, the first sub-circuit being a signal processing unit distinct from the processor integrated circuit, the CPU being arranged to provide a performance dependent on the version number that is stored in the write-protected memory.

6. A circuit module according to Claim 5, wherein the watchdog circuit comprises a register, the circuit module being arranged to write a copy of the version number from the write-protected memory in the register on power up, the watchdog circuit replacing the version number in the command by the version number from the register.

7. A circuit module according to Claim 2, wherein the first sub-circuit is a signal processing circuit having an input and/or output for receiving and/or transmitting input signals to be processed or results of signal processing, the performance determining a processing capacity for processing said signals and/or producing said results, the input and/or output comprising the communication link over which the version number is communicated multiplexed with said input signals and/or results.

8. A circuit module according to Claim 7, wherein the first sub-circuit comprises a control circuit arranged to detect a predetermined time-slot in a predetermined format of the input signal or result and to cause data from the input and/or output that is received during said time slot to be copied to the version memory.

9. A circuit module according to Claim 7, wherein input signal or result is a video signal, the time slot being a blanking period in said video signal.

10. A processor integrated circuit comprising:

- a write-protected memory;
- operating circuits arranged to provide a performance dependent on a version number that is stored in the write-protected memory;
- an external bus input;

- a communication bus output;
- a watchdog circuit coupled between the external bus input and the communication bus output, the watchdog circuit being arranged to pass commands from the external bus input to the communication bus output conditionally, the watchdog circuit detecting whether an update command to update the version number is received and if so to pass said update command, replacing a version number in the update command by a version number from the write-protected memory.

11. A signal processing circuit comprising:
- a version number memory for storing a version number;
- operating circuits arranged to provide a signal processing with a performance dependent on a version number that is stored in the write-protected memory;
- an input and/or output for receiving and/or transmitting input signal to be processed or results of signal processing by said operating circuits;
- a control circuit arranged to detect multiplexed data in a predetermined format of the input signal or result and to cause data from the input and/or output that is received during said time slot to be copied to the version memory.

12. A method of controlling operation of a circuit module, the method comprising
- providing a performance level of a first sub-circuit dependent on the version number that is stored in a version number memory;
- passing a version number from a write-protected memory from a second sub-circuit of the circuit module to the version memory multiplexed with normal operating signals for the first sub-circuit.

13. A method of controlling operation of a circuit module according to Claim 12, the method comprising:
- receiving commands for the circuit module and distributing the commands to the first sub-circuit via a communication bus;
- monitoring received commands for an update command that commands updating of the version number in the version number memory and if so to pass said update command to the communication bus, replacing a version number in the update command by a version number from the write-protected memory.

14. A method of controlling operation of a circuit module according to Claim 12, the method comprising time-slot multiplexing the version number with the input signal to be processed or results of signal processing by said first sub-circuit.

15. A method of controlling operation of a circuit module according to Claim 14, detecting a predetermined time-slot in a predetermined format of the input signal or result and copying data from the input and/or output that is received during said time slot to the version memory.